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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/676,996	09/30/2003	Hyong-ryol Hwang	4591-339	7259

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EXAMINER	
YOHA, CONNIE C	
ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 05/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/676,996	HWANG ET AL.	
	Examiner	Art Unit	
	Connie C. Yoha	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) *27-30 and 34-39* is/are allowed.

6)☐ Claim(s) *1-22, 31-33* is/are rejected.

7)☐ Claim(s) *23-26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Connie C. Yoha

CONNIE C. YOHA
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/30/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office acknowledges receipt of the following items from the Applicant:

Papers submitted under 35 U.S.C. 119(a)-(d) have been placed of record in the file.

Information Disclosure Statement (IDS) filed on 9/30/03 was considered.

2. Claims 1-39 are presented for examination.

Claim Rejections - 35 USC ∋ 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1-22, and 31-33 are rejected under 35 U.S.C. 102(b) as being anticipated by Tobita, Pat. No. 4980799.

With regard to claim 1, Tobita discloses memory device comprising: a core block (fig. 9) including a plurality of sub-arrays (fig. 9, MA1-MA8) and a plurality of sense amplifier regions (fig. 9, SA1-SA8); a plurality of first voltage supply lines (fig. 9, 31) capable of supplying a first operating voltage (fig. 9, VCC or 24) to the plurality of sense amplifier regions; a plurality of second voltage supply lines (fig. 9, 30) capable of supplying a second operating voltage (fig. 9, GND or 29) to the sense amplifier regions; and a charge storing region (fig. 9, the region where capacitor C1-C8 is locate)

arranged at one side of the core block (col. 13, line 30-35) and including charge storing means (fig. 9, C1-C8) connected to the first (fig. 9, 31) and second (fig. 9, 30) voltage supply lines.

With regard to claim 2, Tobita discloses where a sense amplifier (fig. 6, 50) is formed at each of the sense amplifier regions (fig. 9, SA1-SA8), the sense amplifiers being supplied with the first (fig. 9, VCC) and second (fig. 9,, GND) operating voltages.

With regard to claim 3, Tobita discloses where the charge storing means comprises a decoupling capacitor (fig. 6, 34) capable of preventing a power noise (col. 22, line 24-29).

With regard to claim 4, 9-10 and 16-17, Tobita discloses where the decoupling capacitor comprises: an active region (fig. 11, P substrate) formed at one side of the core block); a plurality of first conductive films (fig. 11, 103) formed over the active region (fig. 11, P substrate) and connected to corresponding first voltage supply line (fig. 10A, VCC); and a second conductive film (fig. 11, 103, 113) formed over the active region and connected to the second voltage supply lines (fig. 10A, GND); where the second conductive film is electrically connected to the active region through a plurality of contacts (fig. 11, 109) (also with regard to claim 13, 32 and 33).

With regard to claim 5, Tobita discloses where the plurality of first conductive films is polysilicon forming a gate (fig. 11, 103) (col. 15, line 39-41); and where the second conductive film is a polysilicon forming a bit line (col. 16, line 24-33).

With regard to claim 6, Tobita discloses memory device comprising: a core block (fig. 9) including a plurality of sub-arrays (fig. 9, MA1-MA8) and a plurality of sense

amplifier regions (fig. 9, SA1-SA8) each arranged between sub-arrays; a plurality of first voltage supply lines (fig. 9, 31) capable of supplying a first operating voltage (fig. 9, VCC or 24) to the plurality of sense amplifier regions; a plurality of second voltage supply lines (fig. 9, 30) capable of supplying a second operating voltage (fig. 9, GND or 29) to the sense amplifier regions; and a first charge storing region (fig. 9, the region where capacitor C1 is locate) arranged at one side of the core block (fig. 9, the side of the block MA1), the first charge storing region capable of connecting to the first supply lines (fig. 9, 31); a second charge storing region (fig. 9, the region where capacitor C8 is locate) disposed at another side of the core block (fig. 9, side of the block MA8), the second storing region capable of connecting to the second supply lines (fig. 9, 30).

With regard to claim 7, Tobita discloses where a plurality of sense amplifiers (fig. 9, SA1-SA8) are formed at each of the sense amplifier regions, the sense amplifier being supplied with the first (fig. 9, VCC or 24) and second (fig. 9, GND or 29) operating voltages (also with regard to claim 15).

With regard to claim 8, Tobita discloses where a first charge storing region (fig. 9, the region where capacitor C1 is locate) comprises a first decoupling capacitor (fig. 9, C1); and where a second charge storing region (fig. 9, the region where the capacitor C8 is located) comprises a second decoupling capacitor (fig. 9, C8).

With regard to claim 11, Tobita discloses a row selector circuit (fig. 1, X decoder) disposed adjacent to a side of the core block (also with regard to claim 18).

With regard to claim 12, Tobita discloses a column selector circuit (fig. 1, Y decoder) disposed adjacent to a side of the core block.

With regard to claim 19, Tobita discloses a plurality of third voltage supply lines (fig. 6, line carrying voltage /Θs) disposed on sense amplifier and word line driving regions, capable of supplying the first operation voltage to the sense amplifiers; a plurality of fourth voltage supply lines (fig. 6, line carrying voltage Θs) disposed on sense amplifier and word line driving regions, capable of supplying the second operating voltage to the sense amplifiers.

With regard to claim 20, Tobita discloses where the first (fig. 6, 31) and third voltage supply lines (fig. 6, line carrying voltage /Θs) are intersected and interconnected at the conjunction regions (fig. 6); and where the second (fig. 6, 30) and fourth (fig. 6, line carrying voltage Θs) voltage supply lines are intersected and interconnected at the conjunction regions.

With regard to claim 21, Tobita discloses a third (fig. 6, 22) and fourth (fig. 6, 25) charge storing means connecting to the third (fig. 6, line carrying voltage /Θs) and fourth (fig. 6, line carrying voltage Θs) voltage supply lines, respectively (also with regard to claim 22).

Allowable Subject Matter

4. Claim 23-26 is objected as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record does not show the limitation of said control circuit includes in combination with other features, where the third is a third decoupling capacitor and fourth charge storing means is fourth decoupling capacitor.

5. Claims 27- 30 and 34-39 are allowed.

The prior art of record does not show the limitation of said control circuit includes in combination with other features, a charging storing region arranged to surround the core region and comprising charge storing means connected to the first, second, third and fourth voltage supply lines and that the charge storing means are decoupling capacitor capable of storing a charge.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicants' disclosure. Ihara (5030859) and Komatsu et al (5173875) disclosed a memory device having capacitors connected to plurality of supply lines and voltages.

7. When responding to the office action, Applicants' are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

8. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02 (b)).

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to whose telephone number is (571) 272-1799. The examiner can normally be reached on Mon. - Fri. from 8:00 A.M. to 5:30 PM. The examiner's supervisor, David Nelms, can be reached at (571) 272-1787. The fax phone

number for this Group is (703) 872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-0956.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov Should you have questions on access to the Private Pair system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

C. Yoha

May 2005

CONNIE C. YOHA
PRIMARY EXAMINER